LZ1132BD/LZ1132BM/LZ1132BR

32-Unit High Voltage MOS IC

■ Description

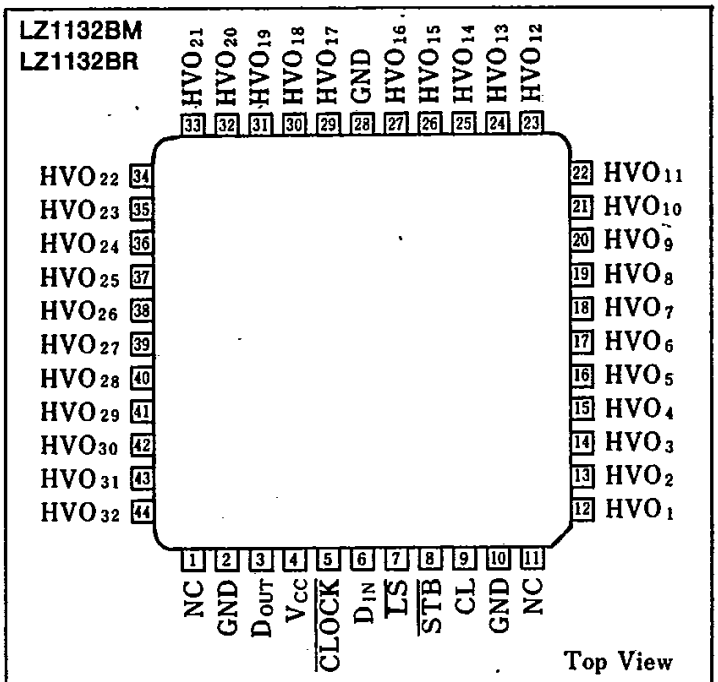
The LZ1132BD/LZ1132BM/LZ1132BR is a 300V 32-output-port monolithic IC fabricated using Sharp's advanced P-channel DMOS process. It can be used as a matrix driver for electroluminescent panels, plasma display panels, electrostatic printers.

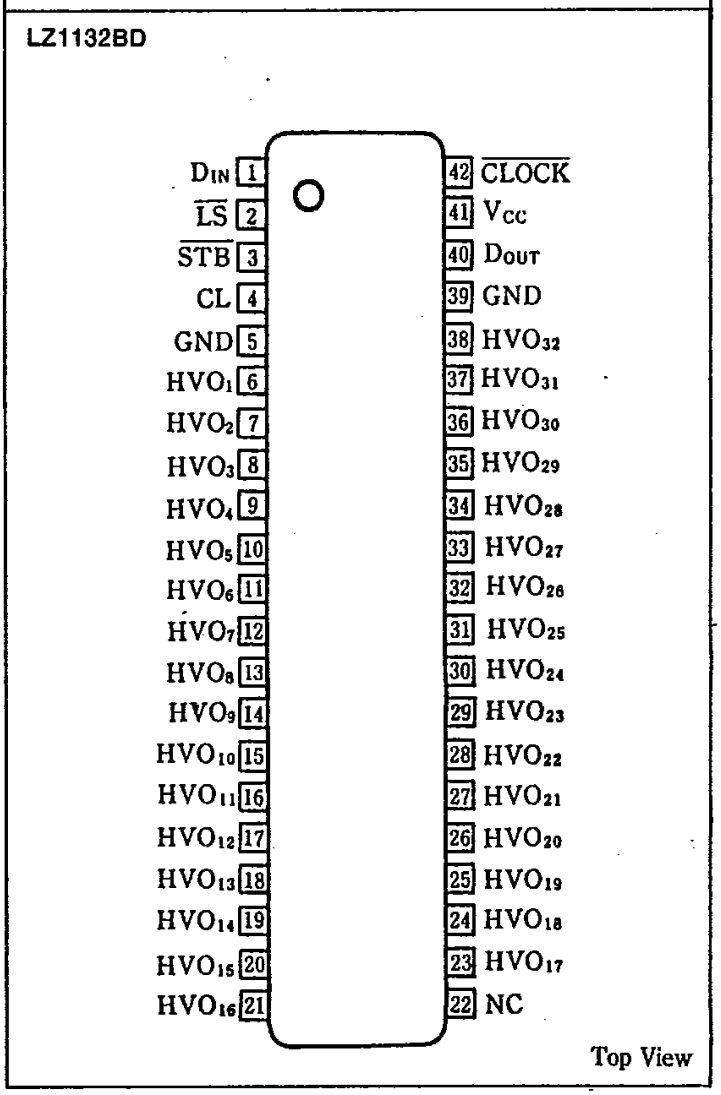
■ Features

1. High voltage output 300 (MIN.)
2. Output current 45mA (TYP.) at V_{HVO}=300V
3. Internal 32-bit shift register circuit
4. Expandable circuit structure
5. High speed data transfer (clock frequency 4MHz)
6. Single power supply : −5V
7. DMOS process
8. 44-pin quad-flat package (LZ1132BM/LZ1132BR*)
   42-pin dual-in-line package (LZ1132BD)

*Reversed bend pin

■ Pin Connections





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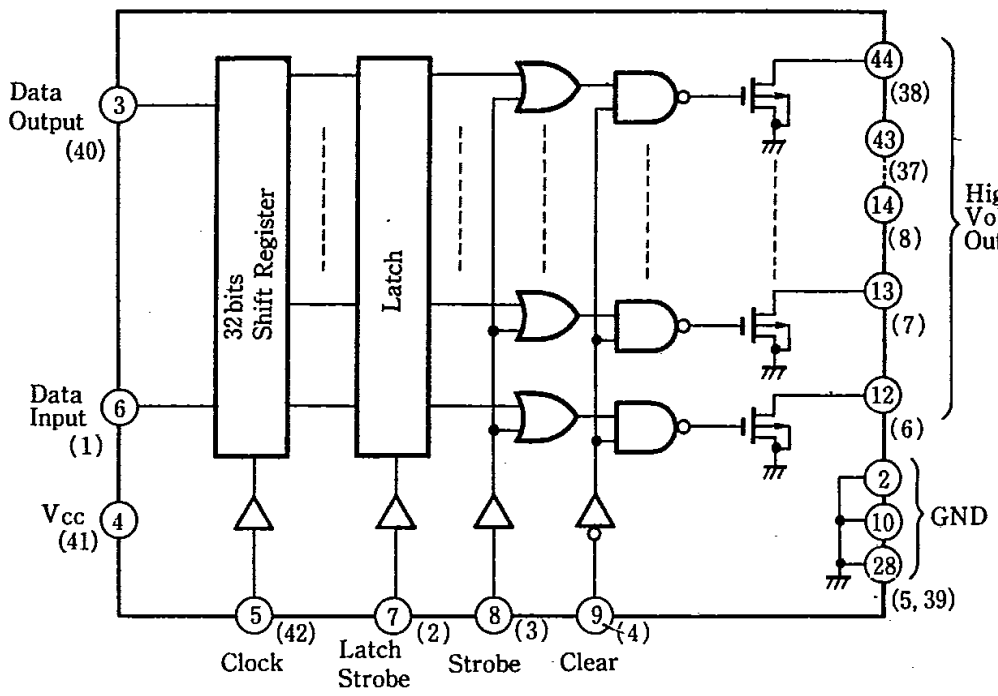
Block Diagram



Truth Table

D_{IN}	CL	$\overline{STB}$	HVMOST
X	H	X	OFF
X	L	H	ON
H	L	L	ON
L	L	L	OFF

(Note) Numbers in paren theses apply to the LZ1132BD.

Absolute Maximum Ratings

(Ta=25℃)

Parameter	Symbol	Conditions	Ratings	Unit	Note
Supply voltage	V_{CC}		−7 to +0.3	V	1
Input voltage	V_{IN}	Applied to all input pins.	−7 to +0.3	V	1
Output voltage	V_{OUT}	Applied to the data output	−7 to +0.3	V	1
	$V_{HVO(ON)}$		−300 to +0.3	V	1,2
	$V_{HVO(OFF)}$		−350 to +0.3	V	1,3
Power consumption	P_D	Ta≦25℃	600	mW	
P_D derating ratio	ΔP_D/℃	Ta>+25℃	5	mW/℃	
Operating temperature	T_{opr}		−20 to +70	℃	
Storage temperature	T_{stg}		−55 to +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: The maximum applicable voltage when HVMOST is ON. D (duty cycle) = 0.1%, ON time = 10 μs
Note 3: The maximum applicable voltage when HVMOST is OFF.

DC Characteristics

(1) HVMOST Characteristics

(V_{CC}=−5V±10%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
ON-state resistance	R_{ON}	HVMOST "ON" I_{HVO}=−1mA, Ta=25℃		1.0	1.3	Ω	
Output current	I_{HVO}	HVMOST "ON" V_{HVO}=−300V, Ta=25℃	−40	−45		mA	1
Output leakage current	$\lvert I_L \rvert$	HVMOST "OFF" V_{HVO}=−300V, Ta=−20 to +70℃			10	μA	2
Total output leakage current	$\lvert I_{TL} \rvert$	HVMOST "OFF" V_{HVO}=−300V, Ta=−20 to 70℃			30	μA	3

Note 1: Duty cycle = 0.1%, ON time = 10 μs
Note 2: Value for each HVMOST output pin.
Note 3: Sum of total output leakage current.

(2) Logic Section Characteristics

(V_{CC}=5V±10%, Ta=−20 to +70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	I_{CC}	V_{IN}=0V		−8	−16	mA
Input "High" voltage	V_{IH}		−0.8		0.3	V
Input "Low" voltage	V_{IL}		V_{CC}		−2.4	V
Output "High" voltage	V_{OH}	I_{OH}=−0.2mA; applied to $\overline{D_{OUT}}$	−0.5			V
Output "Low" voltage	V_{OL}	I_{OL}=1.6mA; applied to $\overline{D_{OUT}}$			−2.5	V
Input leakage current	I_{IL}	V_{IN}=0V to V_{CC}			10	μA

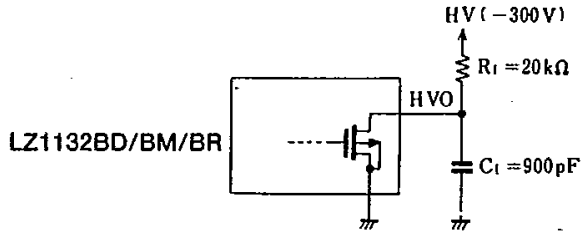
■ AC Characteristics

(V_{CC}=5V±10%, Ta=−20 to +70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock frequency	f_ϕ				4	MHz	
Clock pulse width	t_ϕ, $t_{\overline{\phi}}$		125			ns	
$\overline{D_{IN}}$ setup time	t_{DS}		60			ns	
$\overline{D_{IN}}$ hold time	t_{DH}		60			ns	
LS pulse width	t_{LP}		150			ns	
Clock to LS delay	t_{CL}		0			ns	
LS to clock delay	t_{LC}		0			ns	
$\overline{D_{OUT}}$ delay	t_{PD}	C_L (D_{OUT})=30pF			250	ns	
LS to STB delay	t_{LSB}		0			ns	
LS to $\overline{CL}$ delay	t_{LCL}		0			ns	
STB pulse width	t_{SP}		1			μs	
$\overline{CL}$ pulse width	t_{CLP}		1			μs	
HVO fall time	t_{PL}	C_L (HVO)=900pF, R_L=20kΩ			60	μs	
HVO rise time	t_{PH}	C_L (HVO)=900pF, R_L=20kΩ			15	μs	1

Note 1: Output delay time varies depending on load condition.

Test conditions
- Input rise/fall time: 20 ns
- Time measurement level: 50%
- HVO output load conditions(figure at right).



■ Capacitance

(V_{CC}=0V, f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V		6	10	pF
Output capacitance	C_{HVO}	V_{HVO}=0V		17	30	pF

All pins except pin being measurement are counnected to GND.

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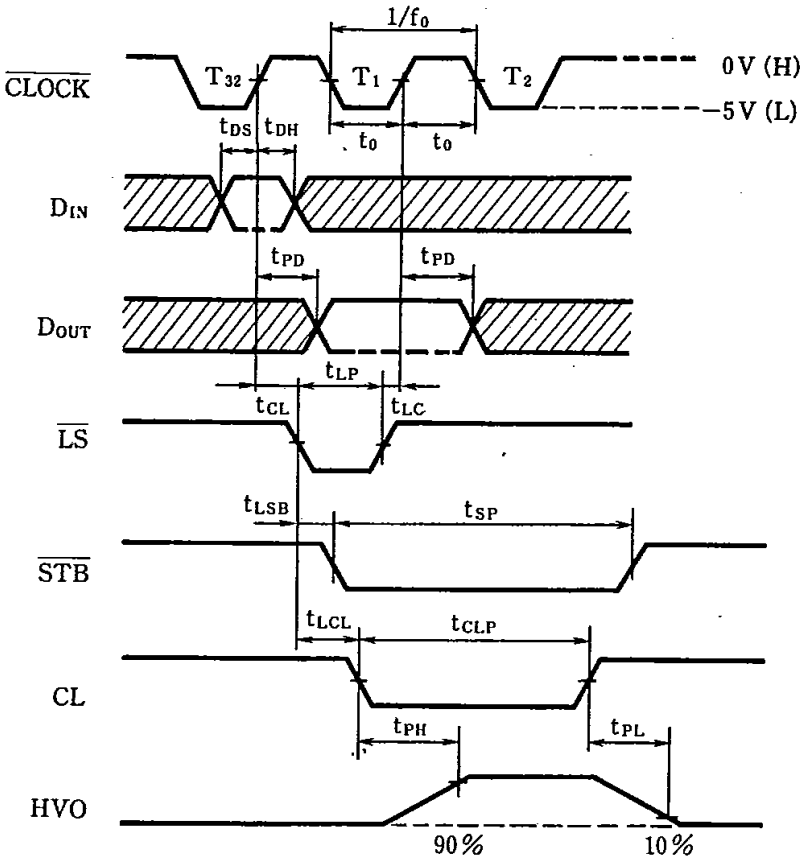
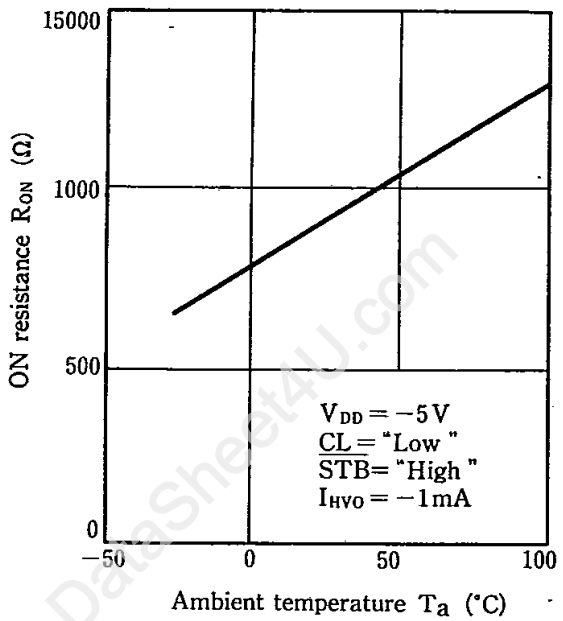
■ AC Timing Diagram

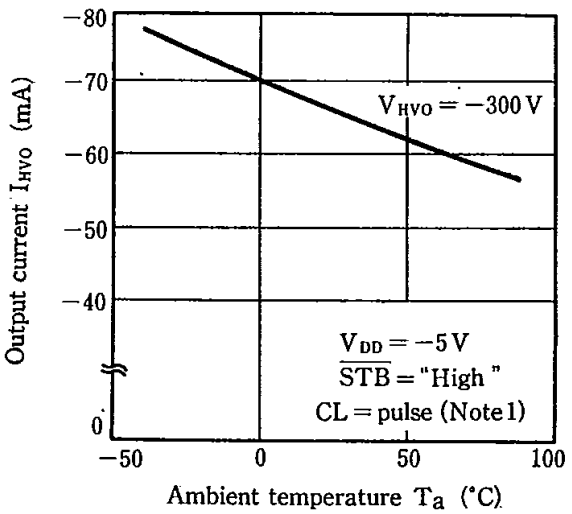


■ Electrical Characteristic Curve

ON resistanse vs. Ambient temperature



Output current vs. Ambient temperature



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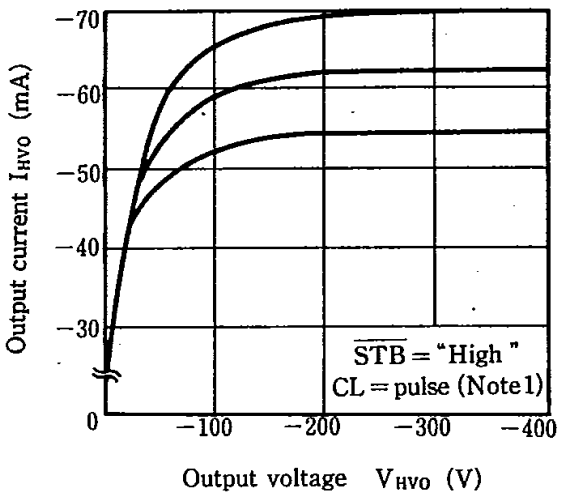
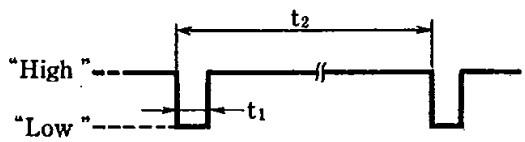
Output current vs. Output voltage



Note1 : Apply below pulse to the CL.



$t_1 = 10\,\mu s$
$t_2 = 10\,ms$
(Duty cycle = 0.1%)